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Transparent Nanotubular Capacitors Based On Transplanted Anodic Aluminum Oxide Templates

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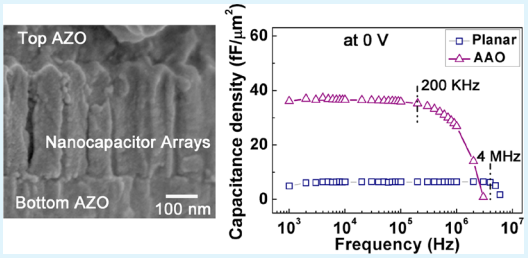
ABSTRACT: Transparent AlZnO/Al_2O_3/AlZnO nanocapacitor arrays have been fabricated by atomic layer deposition in anodic aluminum oxide templates transplanted on the AlZnO/glass substrates. A high capacitance density of 37 fF/μm^2 is obtained, which is nearly 5.8 times bigger than that of planar capacitors. The capacitance density almost remains the same in a broad frequency range from 1 kHz to 200 kHz. Moreover, a low leakage current density of 1.7×10^{-7} A/cm^2 at 1 V has been achieved. The nanocapacitors exhibit an average optical transmittance of more than 80% in the visible range, and thus open the door to practical applications in transparent integrated circuits.



KEYWORDS: *transparent capacitors, atomic layer deposition, anodic aluminum oxide*

INTRODUCTION

In recent years, progresses have been made in development of transparent electronic devices such as flat-panel displays, e-papers, thin film solar cells and see-through computers.[1,2] Transparent circuit technology is of vital importance in the fabrication process of these devices.[3,4] As basic units in transparent circuits, capacitors play an important role such as high-frequency charging and discharging capacitors in active matrix displays,[5,6] decoupling capacitors for microprocessors, filter and analog capacitors working with other electronic components to realize various logical functions.

It is known that high capacitance density means reduced feature size and low power consumption.[7] Many high-k materials, including Al_2O_3,[8,9] HfO_2,[10] TiO_2[11,12] and various hybrid dielectric stacks,[13] have been used in metal−insulator−metal capacitors to increase the capacitance density. However, there are few reports about applications of high-k dielectrics on transparent capacitors. In 2009, Xian et al. fabricated a kind of transparent storage capacitors for solar cells by pulsed laser deposition (PLD). The $Bi_2Mg_{2/3}Nb_{4/3}O_7$ (BMN) dielectric films showed a high dielectric constant of 50−68.[14] However, the 200 nm thickness of BMN films reduced the actual capacitance and the thickness can not be accurately controlled by PLD. In 2014, Ritu Gupta et al. reported a kind of transparent and flexible capacitors using metal wire network as transparent electrodes.[15] This kind of capacitor device showed a high capacitance of 20 μF/cm^2 at 1 Hz. In addition, the sol−gel process is very suitable for large area production at low temperatures. However, the capacitance dropped significantly when the frequency was above 1 Hz, which limited their applications in high-frequency integrated circuits. In our previous work, we demonstrated a kind of transparent capacitors with nanolaminate $Al_2O_3/TiO_2/Al_2O_3$ as dielectrics and Al-doped ZnO (AZO) as electrodes on quartz glass.[16] A maximal capacitance density of 14 fF/μm^2 at 1 kHz was achieved. In addition, the film thicknesses can be precisely controlled by atomic layer deposition (ALD), which is very useful to realize integration in transparent circuits. But on the whole, the capacitance density of current planar capacitors is still not high enough.

To further increase the capacitance value, we should introduce high-aspect-ratio three-dimensional nanostructures into the capacitor structures because they can significantly increase the effective area of electrodes. Among various nanostructures, anodic aluminum oxide (AAO) templates have been widely used because the nanopore arrays exhibit a high degree of regularity and uniformity.[17,18] In addition, the fabrication process is simple and of low-cost. In terms of film deposition methods, ALD has become the leading process used to achieve film coatings with atomic layer accuracy and excellent conformity on internal surfaces of nanostructures with any features. The combination of AAO templates and ALD technology has been an effective way to obtain highly controlled, self-aligned nanocapacitors. In 2009, P. Banerjee et al. demonstrated TiN/Al_2O_3/TiN electrostatic nanocapacitors fabricated on AAO templates. The capacitance density of 10 μF/cm^2 (for 1 μm thick AAO) and 100 μF/cm^2 (for 10 μm thick AAO) was achieved, which is claimed superiority over those previously reported.[19] Such nanocapacitors are very promising for next-generation energy storage, but the TiN electrodes and aluminum (Al) base limit their applications in transparent electronics. To explore the feasibility of fabricating transparent nanocapacitors, we chose AZO to serve as the transparent electrodes.[20−22] The nanocapacitors with AZO

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electrodes reported by L. C. Haspert et al. exhibited excellent electrostatic properties.[22] However, a large sheet resistance of the AZO bottom electrode determines that the bottom electrode contact can only be made on the Al foil, which means that the Al base can not be removed. Thus, the transparency of entire device structures can not be realized.

As an alternative, the AAO template without Al base and barrier layer can be transplanted on any planar substrates through van der Waals force, which provides a solution to applications of AAO on transparent electronics. In this work, free-standing AAO templates were transferred to AZO/glass substrates. Then the entire structures of capacitors (AZO/Al_2O_3/AZO) were in situ grown in the AAO templates by ALD. The in situ grown method can produce sharp and smooth interfaces without outside contaminations, which is very beneficial for performances of nanocapacitors and low-cost mass production. The structural and electrical properties were characterized to evaluate the performances of nanocapacitors. The obtained capacitance and leakage current densities are 37 fF/μm^2 at 10 kHz and 1.7×10^{-7} A/cm^2 at 1 V, respectively. The leakage mechanisms of both planar and AAO capacitors were also investigated.

EXPERIMENTAL METHODS

High-purity (99.999%) aluminum foils were used to fabricate AAO templates through a typical two-step anodizing procedure. According to the anodization conditions, the pore diameter and interpore edge-to-edge distance are expected to be 80 and 20 nm, respectively. The depth of AAO pores is estimated to be 400 nm. After anodization, the aluminum base and barrier layer were removed and the free-standing AAO templates were transferred to AZO/glass substrates. Details of anodization and transferring methods can be found elsewhere.[23] Figure 1 shows the detailed fabricating process of nanocapacitors. First, a small part of AZO was protected by Kapton tape to serve as the probe position during subsequent electrical measurements. Then, the stack of AZO/Al_2O_3/AZO (14.8/10/14.8 nm) was deposited in the AAO template by ALD (Beneq TFS-200), as shown in Figure 1b. The two layers of 14.8 nm thick AZO films served as the bottom and top electrodes of nanocapacitors. The aforementioned AZO and Al_2O_3 film thicknesses were choosed to guarantee that the entire MIM structure can fill up the AAO pores. In addition, the 10 nm thick Al_2O_3 films can achieve a low leakage current and relatively high capacitance density according to the data from planar capacitors. It should be noted that the thin bottom AZO films (14.8 nm) on AAO sidewalls were connected with the thick AZO films (185 nm) on quartz glass. Here, the 185 nm thick AZO films served as the contacting layer of the bottom electrode with a relatively low resistivity of about 2×10^{-3} Ω cm according to the Hall-effect measurement. All AZO films were deposited at 175 °C and consisted of given periods. Each period included 20 cycles of ZnO and 1 cycle of Al_2O_3. Diethyl zinc (DEZn) and deionized water were used as precursors to deposit ZnO films with a growth rate of 0.18 nm/cycle. Al_2O_3 films were grown by using trimethyl aluminum (TMA) and water with a growth rate of 0.1 nm/cycle. The contacting layer included 50 periods with a target thickness of 185 nm. The bottom or top electrode layer each consisted of 4 periods, providing a target thickness of 14.8 nm. The Al_2O_3 dielectric films were deposited at 200 °C. The growth rate is 0.1 nm/cycle and the total cycles are 100. The detailed conditions were the same with that of Al_2O_3 in AZO and can be found in our previous work.[24,25] After that, another AZO films with a thickness of 185 nm were deposited as the contacting layer of top electrodes. The AZO/Al_2O_3 (10 nm)/AZO planar capacitors were also fabricated for comparison. The thicknesses of AZO electrodes of planar capacitors were kept at 185 nm. And the growing conditions of AZO and Al_2O_3 were the same as that of nanocapacitors. Standard photolithography and wet etching process were used to etch the top AZO electrode and contacting layer to form capacitor areas. The final capacitor devices were all about 100 × 100 μm^2 in area. The surface and cross-section of the capacitor devices were characterized by a field-emission scanning electron microscope (FE-SEM, Hitachi S-4800). The capacitance versus voltage ($C-V$), capacitance versus frequency ($C-F$), and leakage current versus voltage ($I-V$) characteristics were measured by a semiconductor device analyzer (Keithley 4200). The optical transmittance was measured by a UV−vis−NIR spectrophotometer (Varian Cary 5000). The resistivity of AZO films was measured by a Hall system (Lakeshore 7700).

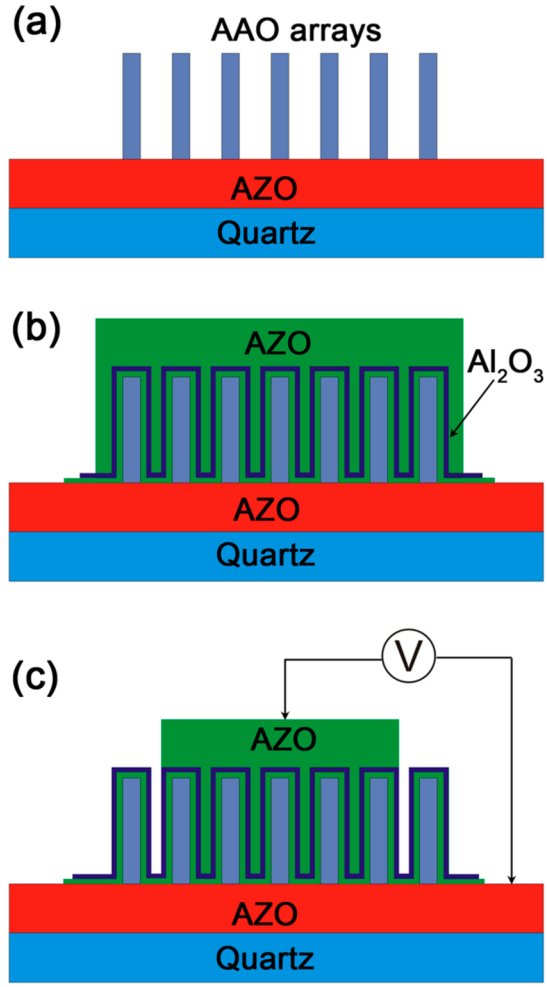

Figure 1. Schematic diagrams of fabricating process for AZO/Al_2O_3/AZO nanocapacitors. (a) Free-standing AAO templates were transferred to AZO/glass substrates. (b) AZO/Al_2O_3/AZO structure and top AZO contacting layer were deposited by ALD. (c) Photolithography and wet etching of the top AZO contacting layer and electrode to define the capacitor area.

RESULTS AND DISCUSSION

Figure 2 shows the optical transmittance spectra of AAO capacitors and the AZO/glass substrate. An average optical transmittance over 80% in the wavelength range from 400 to 800 nm was observed, which is valuable for applications in transparent circuits. As seen from the inset of Figure 2, the characters of Wuhan University can be clearly observed from the device. However, the transmittance of nanocapacitors is a little bit lower than that of the AZO/glass substrate, which is probably due to the incorporation of impurities from AAO templates.

To determine whether the nanocapacitor structures have formed inside the AAO pores, we conducted SEM measure-

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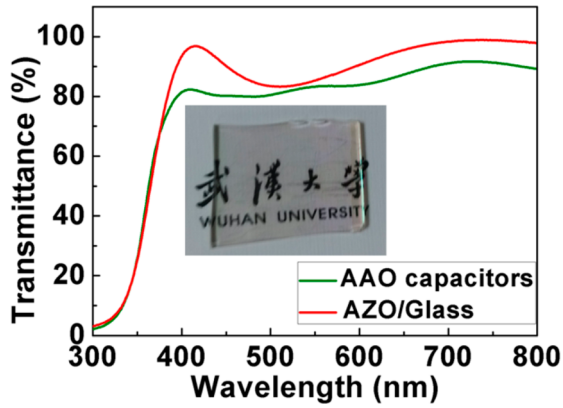

Figure 2. Optical transmittance spectra of the nanocapacitors and AZO/glass substrate. The inset is the photo image of nanocapacitor device with the Chinese characters of "Wuhan University" on the background.

ments. As shown in Figure 3a, the transplanted AAO templates exhibit intact hexagonally arranged and uniform nanopores.

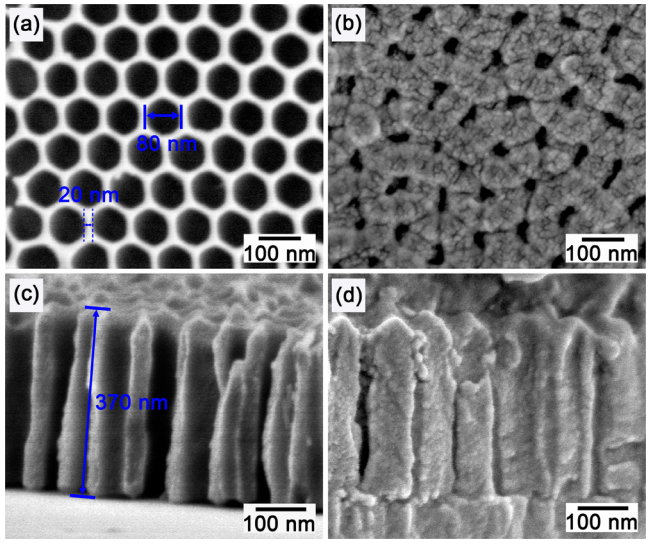

Figure 3. (a) Plan-view SEM image of the transplanted AAO template, showing intact hexagonal unit cells. (b) Plan-view of SEM image after depositing the bottom AZO electrode and Al_2O_3 dielectrics. (c) Cross-sectional SEM image of the transplanted AAO template on silicon wafers, showing many sharp interpore peak asperities on the AAO surface. (d) Cross-sectional SEM image of nanocapacitor arrays, proving the entire capacitor structure have been grown in the AAO templates because of the increased size of nanopillars and fully filled nanopores.

The pore diameter and interpore edge-to-edge distance are measured to be about 80 and 20 nm, respectively. A pore density of about $1.23 \times 10^2/\mu m^2$ is then calculated. After wet etching, the top AZO electrode and contacting layer were removed. As shown in Figure 3b, the diameters of AAO pores were reduced and the interpore edge-to-edge distances were significantly increased, proving that the bottom electrode and Al_2O_3 dielectrics have been grown inside the nanopores. But the shape of the nanopores became irregular, which could be attributed to the relatively large roughness of AZO films deposited on sidewalls of AAO. Figure 3c shows the cross-sectional images of the AAO templates transplanted on silicon wafers. The sharp interpore peak asperities on the AAO surface are observed and each peak corresponds to an interpore pillar. Here, the interpore pillar can be regarded as a basic unit of the AAO template for convenience of subsequent analysis. Figure 3d shows the cross-sectional images of nanocapacitor arrays. The pores were finally fully filled after deposition of the top AZO electrode and contacting layer. In addition, the width of the interpore pillar was increased significantly, which proves that the nanocapacitor arrays have been fabricated successfully inside the AAO pores. Moreover, it is worth mentioning that the small gaps between the AAO template and AZO/glass substrate have been filled by the bottom AZO films because of the unique growth mode of ALD.

Figure 4 shows the $C-V$ characteristics of capacitors formed on planar and AAO substrates. Here, 10 kHz and 1 MHz were selected as representatives of low and high frequencies, respectively. As shown in Figure 4a, the capacitance density of planar capacitors is about 6.4 $fF/\mu m^2$ at 0 V, corresponding to a dielectric constant of 7.2, which is close to that of Al_2O_3 materials. The capacitance density of nanocapacitors reaches 37 $fF/\mu m^2$ at 0 V, which is nearly 5.8 times larger than that of the planar capacitors. Furthermore, the total capacitance density (C_{total}) of nanocapacitor arrays can be estimated by the following eqs 1−4[19]

$$C_{total} \approx \alpha(C_{top} + C_{pore} + C_{bottom}) \quad (1)$$

$$C_{top} = \frac{\varepsilon_r \varepsilon_0}{t_{insulator}}\left[\frac{\sqrt{3}}{2}(2r_{pore} + D)^2 - \pi r_{pore}^2\right] \quad (2)$$

$$C_{pore} = \frac{2\pi\varepsilon_r\varepsilon_0 L}{\ln\left(\frac{r_{pore} - t_{BE}}{r_{pore} - t_{BE} - t_{insulator}}\right)} \quad (3)$$

$$C_{bottom} = \varepsilon_r\varepsilon_0\pi\frac{(r_{pore} - t_{BE} - t_{insulator})^2}{t_{insulator}} \quad (4)$$

Here, C_{top}, C_{pore}, and C_{bottom} represent capacitance densities of the top interpore part, the sidewall area and the bottom part of one single AAO pore, respectively. α represents the pore density, which is about $1.23 \times 10^2/\mu m^2$ according to direct SEM measurement. ε_r is the relative dielectric constant of Al_2O_3, which is 7.2 according to calculated results of the planar capacitors. ε_0 is the vacuum dielectric constant. t_{BE} and $t_{insulator}$ correspond to the thicknesses of bottom AZO electrode and Al_2O_3 dielectrics, which are 14.8 and 10 nm, respectively. L and r_{pore} represent the depth and radius of AAO pores, which are 370 and 40 nm, respectively. D is the interpore edge-to-edge distance, which is 20 nm. Therefore, the calculated C_{top}, C_{pore}, and C_{bottom} are 2.317×10^{-2}, 0.290, and 4.502×10^{-3} fF, respectively. Hence, the total capacitance density is 39.1 $fF/\mu m^2$, which is in close agreement with the measured result (37 $fF/\mu m^2$). However, it should be noted that the capacitance density decreases gradually when the voltage is varied from negative to positive bias. One possible explanation could be described by the following details. During anodization process, positive ions move toward the aluminum oxide-electrolyte interface while negative ions move toward the aluminum oxide-Al base interface. These ions are likely remaining trapped in the sidewalls of AAO.[26,27] Hence, the positive ions could become mobile and enter the bottom AZO films on AAO sidewalls under a positive bias added on the bottom electrode. These positive ions can produce some inherent electric dipoles which

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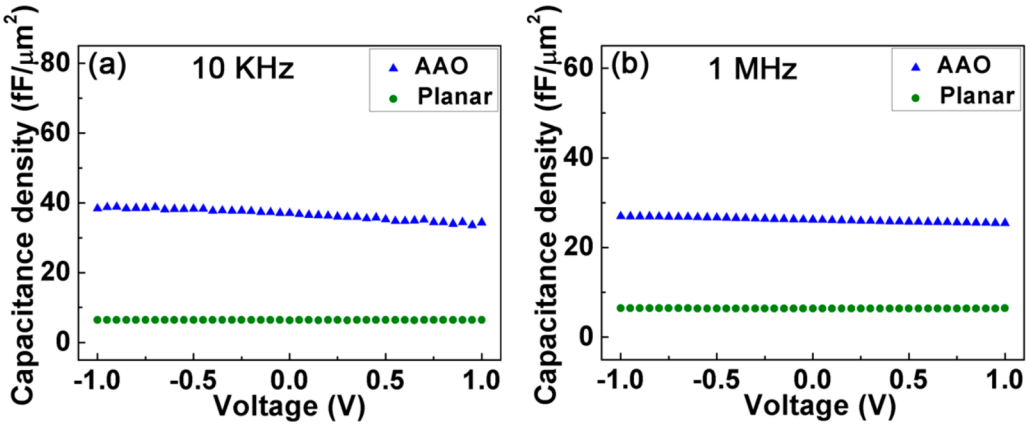

Figure 4. $C-V$ characteristics of AAO and planar capacitors at (a) 10 kHz and (b) 1 MHz. The bottom AZO contacting layer is maintained at 0 V. The voltage added on the top AZO electrode with an area of 100 μm × 100 μm is varied from −1 to 1 V.

will respond to the extra electric field under low frequencies. Hence, the measured capacitance density is increased. This conclusion can be verified by the $C-V$ results measured at 1 MHz. As shown in Figure 4b, the difference of capacitance density at positive and negative bias becomes less obvious when the frequency is increased to 1 MHz. This is because the electric dipoles from impurities have no ability to keep pace with the variation of high-frequency signals.

Figure 5 shows the $C-F$ characteristics of the planar and AAO capacitors at 0 V. According to dielectric theory, dielectric

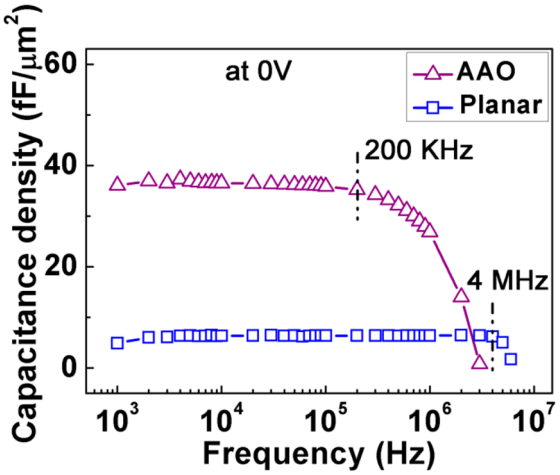

Figure 5. $C-F$ characteristics of AAO and planar capacitors. The DC voltages added on both the top and bottom electrodes are maintained at 0 V. The frequency is varied from 1 kHz to 10 MHz.

loss is proportional to fR_s at high frequencies and inverse proportional to fR_p at low frequencies, where R_s represents the series resistance of electrodes and R_p is the parallel resistance of dielectrics. f is the frequency of alternating voltage added on capacitors. As shown in Figure 5, the planar capacitors have a constant capacitance density of 6.4 fF/μm^2 at a frequency range from 1 kHz to 4 MHz. The drop of capacitance happens when the frequency is above 4 MHz, which is thought to be mainly caused by the relatively big resistivity of AZO (about 2×10^{-3} Ω.cm) comparing with the ordinary metal electrodes. For AAO capacitors, the capacitance density drops significantly when the frequency exceeds 200 kHz. On the basis of the above analysis, this phenomenon is mainly caused by the much larger sheet resistance of the bottom AZO films on AAO sidewalls due to the small thickness (14.8 nm).

Figure 6 shows the $I-V$ characteristics of AAO and planar capacitors. The leakage current density of AAO capacitors is 1.7

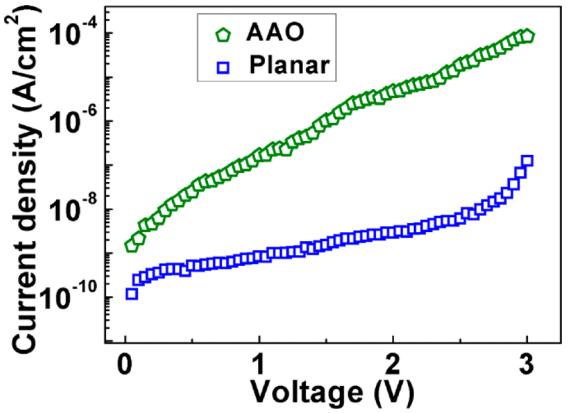

Figure 6. $I-V$ characteristics of AAO and planar capacitors.

× 10^{-7} A/cm^2 at 1 V, which is much larger than that of planar capacitors (8.4×10^{-10} A/cm^2 at 1 V). The increase of leakage current partly results from the enlargement of surface area of dielectrics and some defects which can induce the local electrical short circuits. On the other hand, the structural features of nanocapacitor arrays are also an important factor. Hence, it is necessary to explore the leakage mechanism. Here, Schottky emission and Fowler-Nordheim (F−N) tunneling[28] are used to analyze the conduction mechanisms. Among them, Schottky emission is suitable for low or moderate electric fields. If the Schottky emission exists at a constant temperature, the relationship of ln J vs $E^{1/2}$ should be linear. And the relative dielectric constant can be calculated according to the equation: $kT\beta_s = (e^{3/4}\pi\varepsilon_r\varepsilon_0)^{1/2}$, where β_s represents the slope of ln $J \approx E^{1/2}$ and ε_r is the fitted relative dielectric constant, k is the Boltzmann constant and T is the temperature. Figure 7a shows the Schottky plots of the leakage current with ln $J \approx E^{1/2}$. For AAO capacitors, a linear relationship is observed when the field is below 1.5 MV/cm. The fitted dielectric constant is 5.15, which is reasonable comparing with our measured result (ε_r = 7.2). It should be noted that the fitted dielectric constant is the dynamic one and should be a little smaller than the measured static dielectric constant. Hence, the conduction mechanism of

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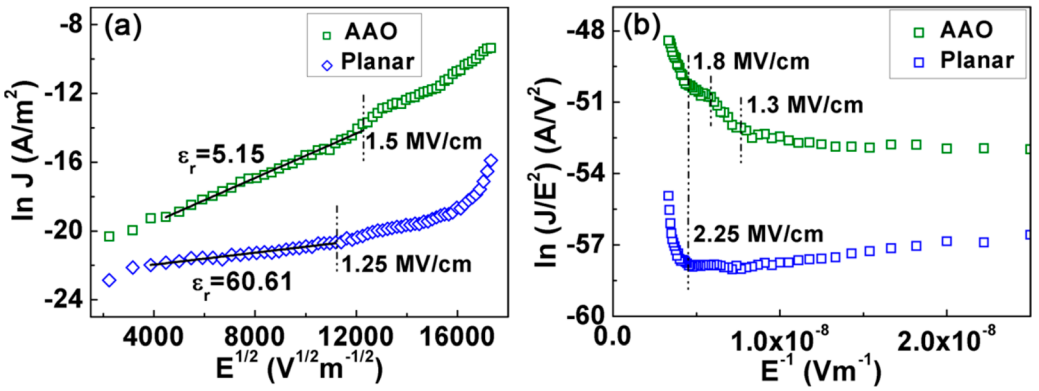

Figure 7. *I*–*V* analysis for AAO and planar capacitors. (a) Schottky plots. (b) F–N tunneling plots.

AAO capacitors is governed by Schottky emission in the low field range (E < 1.5 MV/cm). However, the fitted dielectric constant for planar capacitors is not available (ε_r = 60.61) although a linear relationship is observed when the field is below 1.25 MV/cm. This suggests that the Schottky emission exists but is not the main leakage mechanism for planar capacitors. To explain the difference of leakage mechanism between planar and AAO capacitors, a model is proposed, as shown in Figure 8. The bottom AZO films grown on sidewalls

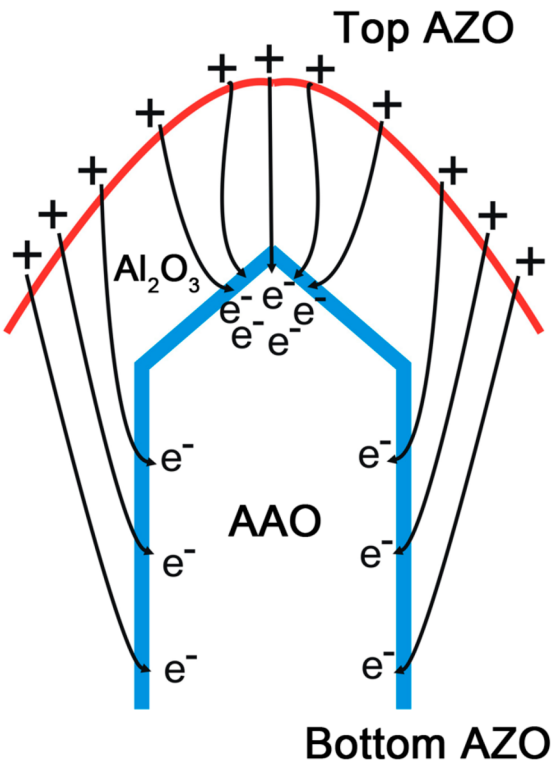

Figure 8. Schematic diagram proposed to explain the Schottky emission at interpore peaks of nanocapacitors.

of AAO will be negatively charged when a positive voltage is added on the top AZO electrode. The electrons in bottom AZO films will gather on the sharp peaks of AAO pillars because of their small radius of curvature. The accumulated electrons can lead to a local high electric field which will enhance the field-assisted emission. Therefore, Schottky emission dominates the leakage mechanism of AAO capacitors in the low field range. F–N tunneling is usually used to describe the conduction mechanism in the high field range. The relationship between $\ln(J/E^2)$ and E^{-1} should be linear if the F–N tunneling exists. Figure 7b shows the F–N plots with $\ln(J/E^2) \approx E^{-1}$. For planar capacitors, a linear relationship is observed when the field is above 2.25 MV/cm. However, for AAO capacitors, there are two sections with linear relationships, which suggests that F–N tunneling happens in two field ranges. F–N tunneling exists in the field range from 1.3 to 1.8 MV/cm (section 1) mainly because the local high electric field enhances the tunneling probability of electrons in the sharp peaks of AAO nanopillars. When the field is above 2.25 MV/cm (section 2), all electrons in bottom AZO have bigger probabilities to tunnel the Al_2O_3 barrier layer, which suggests that the F–N tunneling is the result of both the extra electric field and the local enhanced electric field. Hence, there exists an inflection point between the two sections.

CONCLUSIONS

In conclusion, we have successfully fabricated transparent nanocapacitors in transplanted AAO templates by ALD method. *C*–*V* measurements show a high capacitance density of 37 fF/μm^2 at 10 kHz, which is nearly 5.8 times bigger than that of planar capacitors. The capacitance drops significantly when the frequency exceeds 200 kHz, which can be ascribed to the large sheet resistance of thin AZO films grown on AAO sidewalls. By analyzing the leakage mechanisms, we conclude that Schottky emission is the main mechanism in the low field range (E < 1.5 MV/cm) because of the existence of a local high field in sharp interpore peak asperities on AAO surface. In addition, the local high field also leads to a relatively low field (1.3 MV/cm), above which F–N tunneling happens.

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Notes

The authors declare no competing financial interest.

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